REMARKS

Applicant has carefully studied the outstanding Official Action. The present response is intended to be fully responsive to all points of rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Claims 20, 22-23, 26-28, 34, 38-45, 48, 52-55, 59-61 and 63-64 stand rejected under 35 USC 102(a) as being anticipated by Salatino et al (US 5,915,168). Claims 24, 33, 36, 47, 49-50 and 56-58 stand rejected under 35 USC 103(a) as being unpatentable over Salatino and further in view of Ichikawa et al (US 5,996,199). Claims 51 and 65-67 stand rejected under 35 USC 103(a) as being unpatentable over Salatino and further in view of Chen (US 6,083,766).

Salatino describes a wafer level hermetically packaged integrated circuit. Ichikawa describes a method for manufacturing surface acoustic modules. Chen describes a packaging method of thin film passive components on silicon chip employing a ceramic or glass substrate mounted with the silicon chip so as to improve the mechanical strength of the components.

Applicant has amended claim 20 to recite additional features of the present invention. Support for the amendments to claim 20 can be found in the attached annotated version thereof. Applicant notes that the paragraph numbers contained in the annotated version of the claims refer to the paragraph numbers of the application as published.

Applicant respectfully submits that none of the prior art, either alone or in combination, shows or suggests a method of producing a crystalline substrate based

device including providing a wafer including a semiconductor substrate and comprising a plurality of semiconductor microstructures including at least one optoelectronic device, providing at least one wafer-level transparent packaging layer, forming onto said at least one wafer-level transparent packaging layer, a wafer-level spacer, said packaging layer and said spacer defining a plurality of cavities extending entirely through said spacer, sealing said wafer-level spacer to said semiconductor substrate, thereby fully defining a gap between ones of said plurality of microstructures and corresponding chip scale portions of said at least one transparent packaging layer, without requiring removal of material from said at least one transparent packaging layer overlying said at least one optoelectronic device and subsequently dicing said semiconductor substrate, having said wafer-level spacer and said at least one wafer-level transparent packaging layer sealed thereunto, to form individual chip scale packaged devices, as recited in amended claim 20. Applicant respectfully submits that claim 20 is therefore deemed to be allowable.

Applicant has amended claims 39 and 65 to depend from claim 20. Applicant has also amended claims 22-24, 27-28, 33-34, 36, 40-42, 44-45, 47-50 and 67 to provide proper antecedent basis to all elements claimed therein in light of the amendments to claim 20.

Claims 26, 29, 38, 43, 46, 51-64 and 66 have been cancelled without prejudice. Claim 1-19, 21, 25, 30-32, 35 and 37 were previously cancelled.

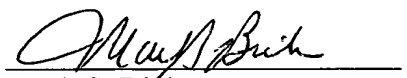
Claims 22-24, 27-28, 33-34, 36, 39-42, 44-45, 47-50, 65 and 67 depend directly or ultimately from claim 20 and recite additional patentable matter and are therefore deemed allowable.

Applicant has carefully studied the remaining prior art of record herein

and concludes that the invention as described and claimed in the present application is neither shown in nor suggested by the cited art.

In view of the foregoing remarks, all of the claims are believed to be in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Respectfully submitted,



Mark S. Bicks
Reg. No. 28,770

Roylance, Abrams, Berdo & Goodman, L.L.P.
1300 19th Street, N.W.
Suite 600
Washington, DC 20036
(202)659-9076

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ANNOTATED VERSION OF AMENDED CLAIM 20

20. (Currently Amended) A method of producing a crystalline substrate based device comprising:

providing a wafer including a semiconductor substrate and comprising a plurality of semiconductor microstructures including at least one optoelectronic device; [Fig. 5B, paragraph 55]

providing at least one wafer-level transparent packaging layer; [Fig. 4A]

forming onto said at least one wafer-level transparent packaging layer, a wafer-level spacer, said packaging layer and said spacer defining a plurality of cavities extending entirely through said spacer; [Figs. 4A-4E, paragraphs 51 and 52]

sealing said wafer-level spacer to said semiconductor substrate, thereby fully defining a gap between ones of said plurality of microstructures and corresponding chip scale portions of said at least one transparent packaging layer, without requiring removal of material from said at least one transparent packaging layer overlying said at least one optoelectronic device; and [Figs. 5A-5B, paragraphs 54 and 55]

subsequently dicing said semiconductor substrate, having said wafer-level spacer and said at least one wafer-level transparent packaging layer sealed thereunto, to form individual chip scale packaged devices. [Fig. 5I, paragraph 57]